



3A 6000

2024 07



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3.2

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4.3 0x0010

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4.4 0x0020

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4.5 0x0180

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4.6

0x0188

4.7

0x0190

4.10

0x01D0

4.14

0x0428

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4.15 SRAM

0x0430

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4.16 FUSE0

0x0460

-

4.17 FUSE1

0x0470

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5.1

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5.2

5.2.1

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5.2.2

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5.3

5.3.1

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5.3.2

5.4 HT

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6.1 Stable Counter

6.1.1 Stable Counter

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6.1.2 Stable Counter

6.2 Node Counter

6.2.1

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6.3

7 GPIO

7.1 0x0500

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7.2 0x0508

-

7.3 0x0510

-

7.5 GPIO

8 LA 664

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8.1 3A 6000

8.2 3A6000

9 Cache SCache

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10.1

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10.2

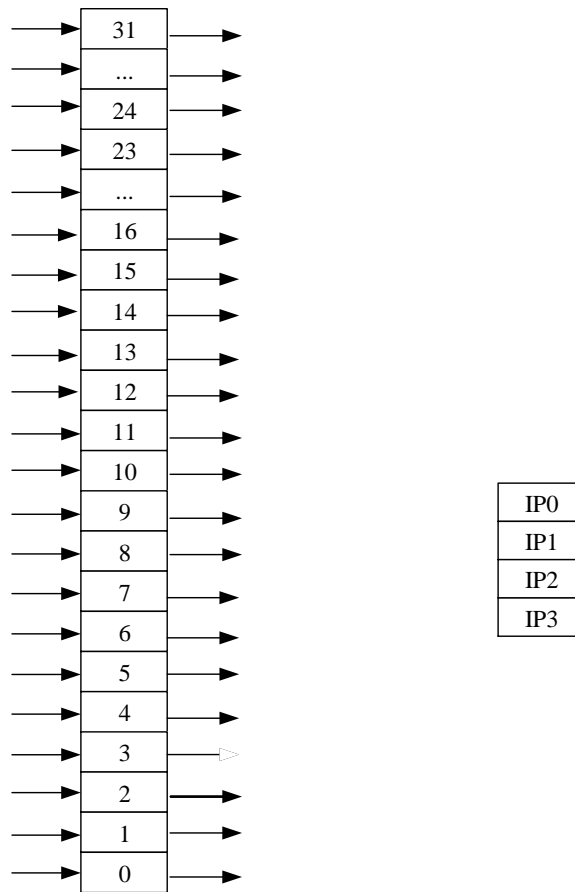
10.3

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11 I/O

11.1 I/O





11.1.1

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11.2.1

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11.2.2

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11.2.3 IO

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11.2.4 IO HT

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12.1

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12.2



12.5

13 DDR4 SDRAM

13.1 DDR4 SDRAM

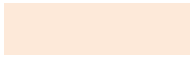
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13.2 DDR4 SDRAM

13.2.1

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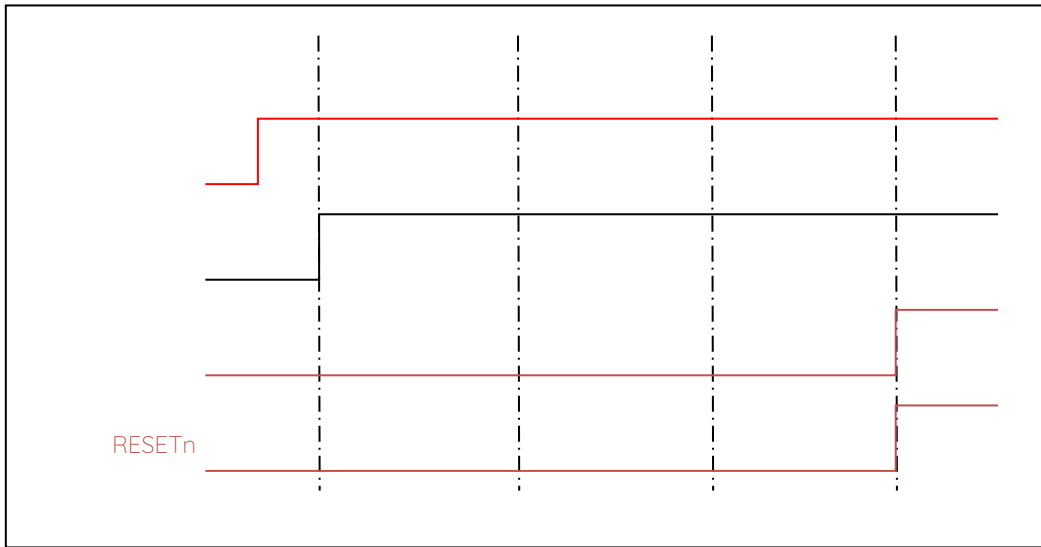


13.3

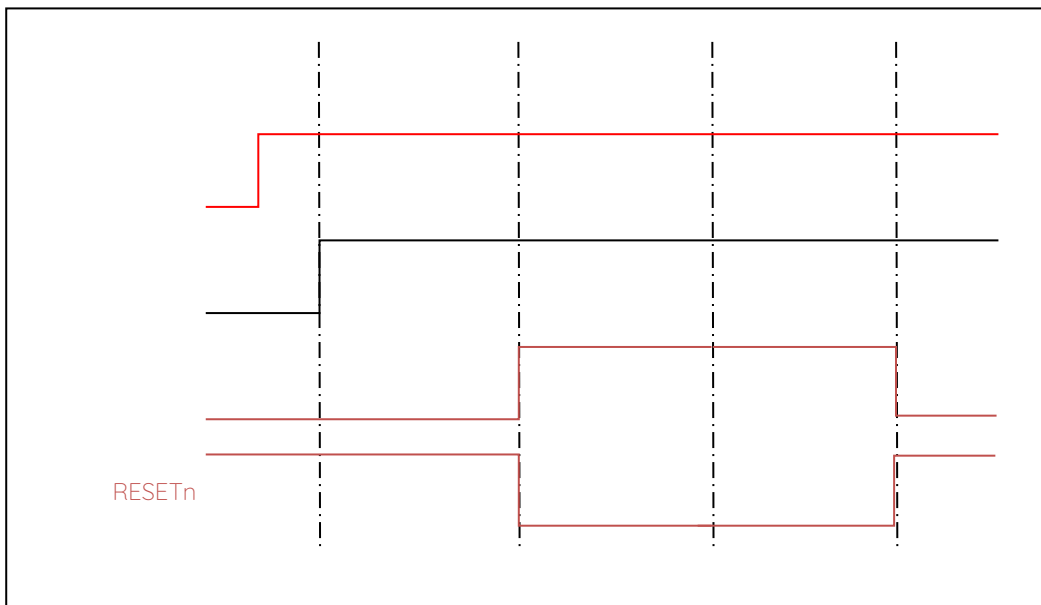
13.3.1

13.3.2

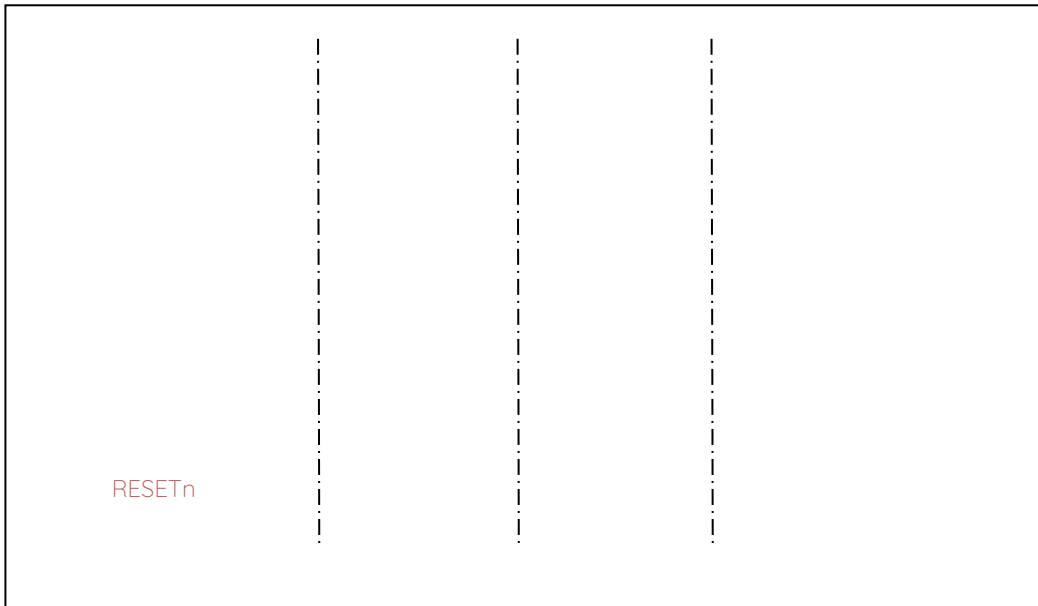
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13.3.3 Leveling

13.3.3.1 Write Leveling

13.3.3.2 Gate Leveling

13.3.4 IO

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13.3.8 ECC

14 HyperTransport

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14.1 HyperTransport

14.2 HyperTransport

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14.3 HyperTransport

14.3.1 PIC

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14.3.3

14.4 HyperTransport

14.4.1 HyperTransport

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14.4.2 HyperTransport

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14.5.1 Bridge Control

14.5.2 Capability Registers



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14.5.3 Error Retry

14.5.4 Retry Count

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14.5.5 Revision ID

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14.5.6 Interrupt Discovery & Configuration

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14.5.7

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14.5.8



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14.5.9 Link Train

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14.5.10

14.5.11

14.5.12 POST



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14.5.13

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14.5.17

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14.5.18 PHY

14.5.19

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14.5.20

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14.5.24 Training 0

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14.5.25 Training 1

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14.5.26 Training 2

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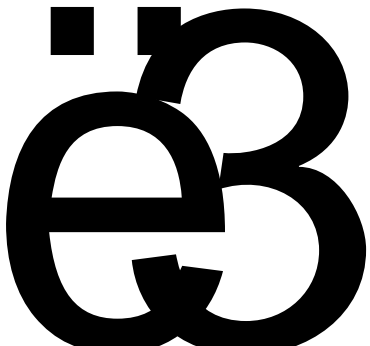
14.5.30 PHY

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14.5.36 Bist

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14.5.39 PHY

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14.5.40 Unitid

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14.5.41 PHY

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14.5.42 PHY

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14.5.43 PHY

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14.5.44 PLL

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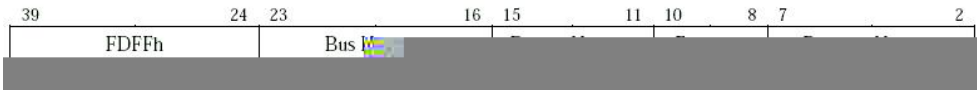
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14.5.46

14.6 HyperTransport

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15 IO

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15.1.1 DAT

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PRERhi				

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CTR	

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